Characterization and Compensation of High Speed Digitizers

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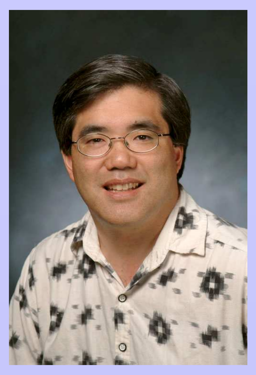
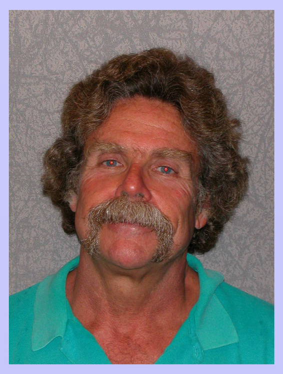




Abstract:

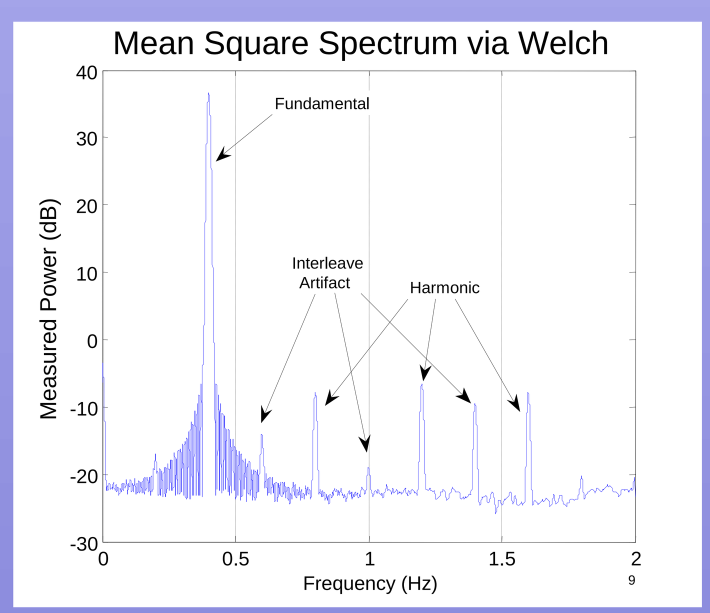
Increasingly, ADC technology is being pressed into service for single-shot instrumentation applications that were formerly served by vacuum-tube based oscilloscopes and streak cameras. ADC technology, while convenient, suffers significant performance impairments. Thus, in these demanding applications, a quantitative and accurate representation of these impairments is critical to an understanding of measurement accuracy. We have developed a phase-plane behavioral model, implemented it in SIMULINK and applied it to interleaved, high-speed ADCs (up to 4 gigasamples/sec). We have also developed and demonstrated techniques to effectively compensate for these impairments based upon the model.

Motivation:

- Analog digital converter (ADC) based digitizers are commonly used to measure high speed transients
- Displacing vacuum tube based scopes or streak cameras due to wide spread commercial support and availability
- Used on large scale, complex, *single-shot*, and expensive science experiments
- Model needed for:
  - Predictive simulation of ADC impairment impact
  - Correction of impairment effects

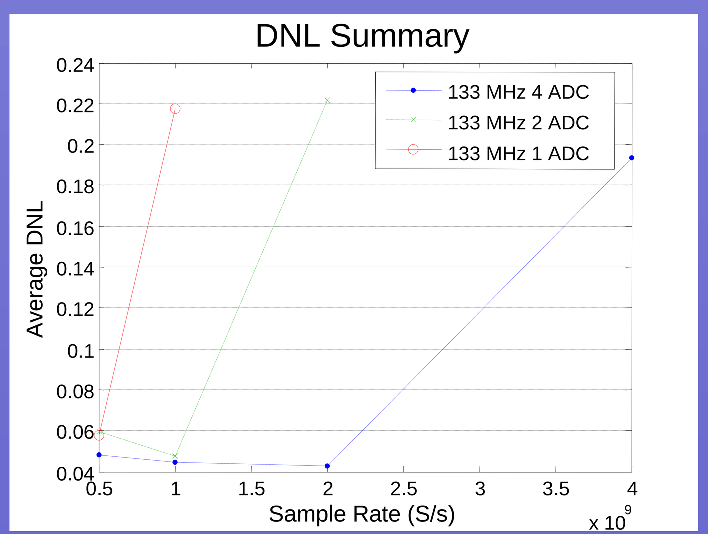
Real World Digitizer Impairments:

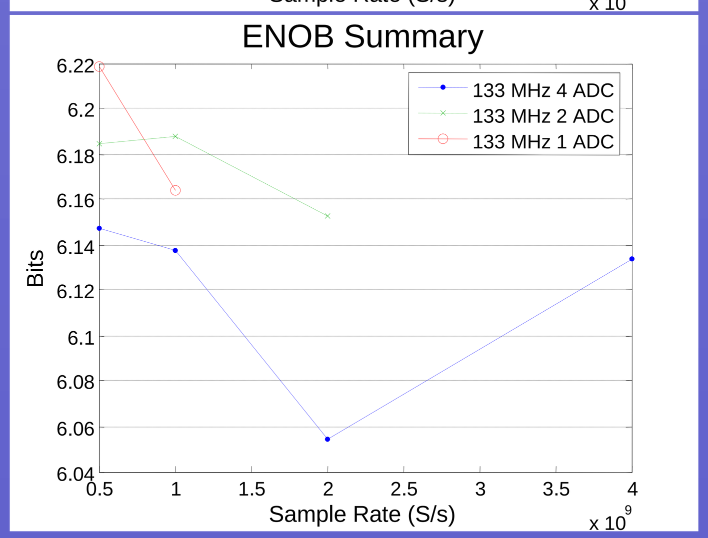
- Time independent
  - Fixed Pattern:
    - Non-linearities in the transition levels (harmonic)
  - Random:
    - Amplitude Noise
- Time dependent
  - Fixed Pattern:
    - Interleaving effects
      - Non-ideal time offset
      - Gain and offset differences
      - Transition level differences
  - Random:
    - Timing jitter
- Possible to compensate for fixed pattern effects



Impairment Sample Rate Dependence:

- Differential Nonlinearity (DNL) improves as sample rates of individual ADCs decrease
- ENOB (Effective Bits) improves as sample rate decreases
- But, fewer ADCs at higher sample rates are better than more ADCs at lower sample rates
- Interleave effects outweigh DNL improvement





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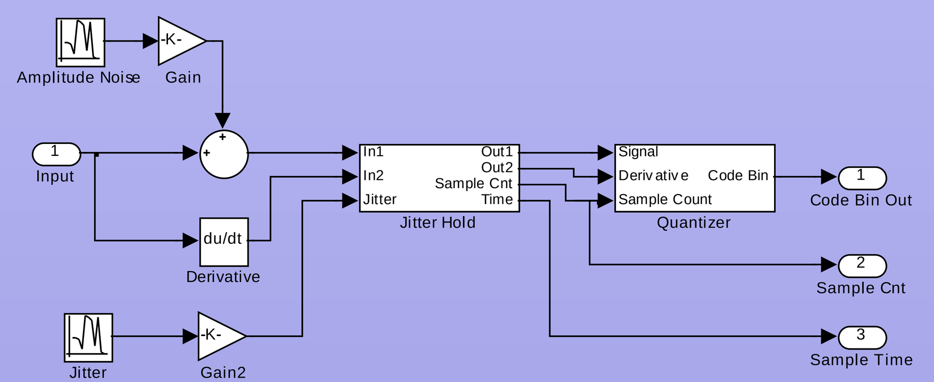
Digitizer Model:

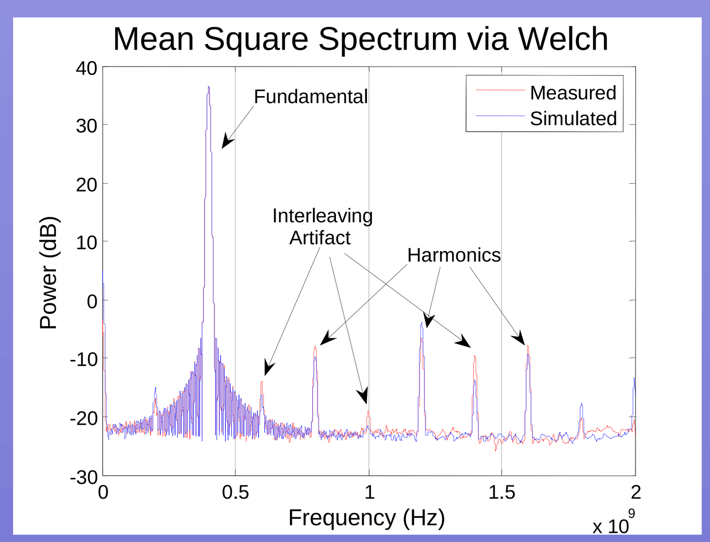
- Two main parts in commercial digitizers
  - Analog front end
    - Scales, offsets, conditions, etc. input
  - One or more ADCs
    - Interleaved for higher effective sample rates
  - Internal design is typically not known to users
- Use a behavior-based model
  - Minimizes need of prior knowledge of inner workings
  - Generally applicable to many designs
- Phase Plane Models
  - Model behavior as function of input signal levels and slopes

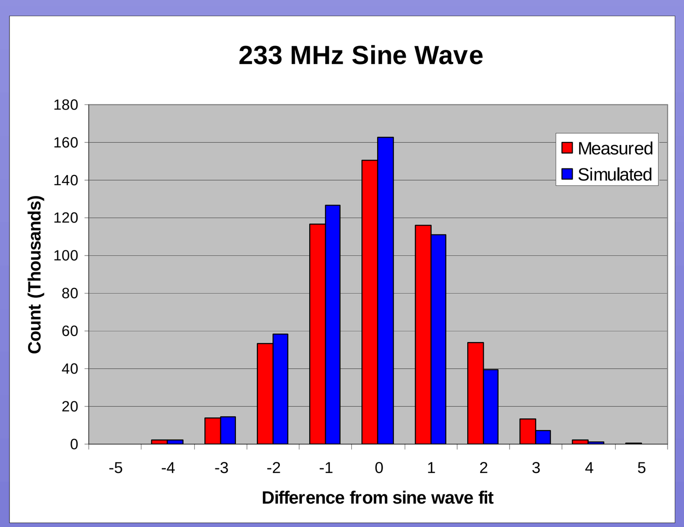


Model diagram in Simulink

Impairments in Simulation:

- Validated model by comparing simulation with collected data
- Model parameters set using sine wave records of an Acqiris DC271 4 GS/s digitizer
  - Transition levels extracted via histogram method (IEEE Std 1057)
  - Noise amplitude set to match noise floor of spectrum
  - Sine waves near 30, 60, 125, 250, and 400 MHz at 7.9, 10.9, 13.9, 16.9, and 19.9 dBm
    - Generated by Agilent E8247C low noise signal generator
    - Filtered with K&L Microwave tunable bandpass filters





Simulation results of 233 MHz sine wave

Compensation of Impairments:

- Transition Level (TL) Compensation
  - Replace each code with the mid-point between it's slope interpolated transition level (Larrabee et al 1998)

$$x[t]=k$$

$$\hat{x}[t]=\frac{T[k,s]+T[k+1,s]}{2} \quad s=\frac{\hat{x}[t]-\hat{x}[t-\Delta t]}{\Delta t}$$

- Independent Transition Level (ITL) Compensation
  - Extend TL to use independent transition levels for each interleaved ADC
- Interleave (Int) Compensation
  - Estimate gains, amplitude offsets, and time offsets for each ADC from reference signals
  - In test signal (Elbornsson, Gustafsson, and Eklund 2004):
    - Subtract amplitude offsets
    - Divide by normalized gains
    - Interpolate to ideal time base
- Transition Level and Interleave (TL + Int) Compensation
  - Perform TL compensation followed by Int compensation

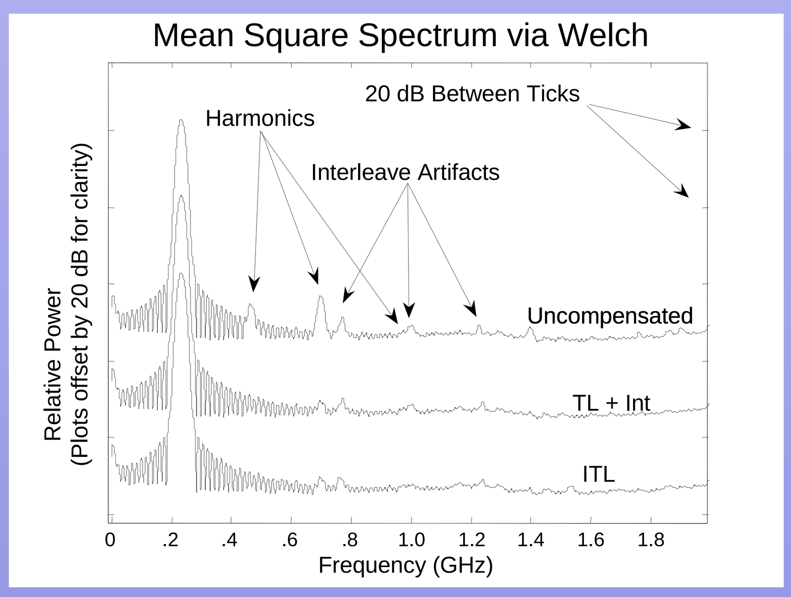
Related Work:

- Phase Plane Modeling and Compensation
  - Larrabee, Irons and Hummels 1998, Acunto, Arpaia, Hummels, and Irons 2001, and Bergman 2003
- Time Interleaved System Modeling
  - Theoretical Model: Vogel 2003
  - Compensation: Elbornsson, Gustafsson, and Eklund 2004 and Jin and Lee 2000

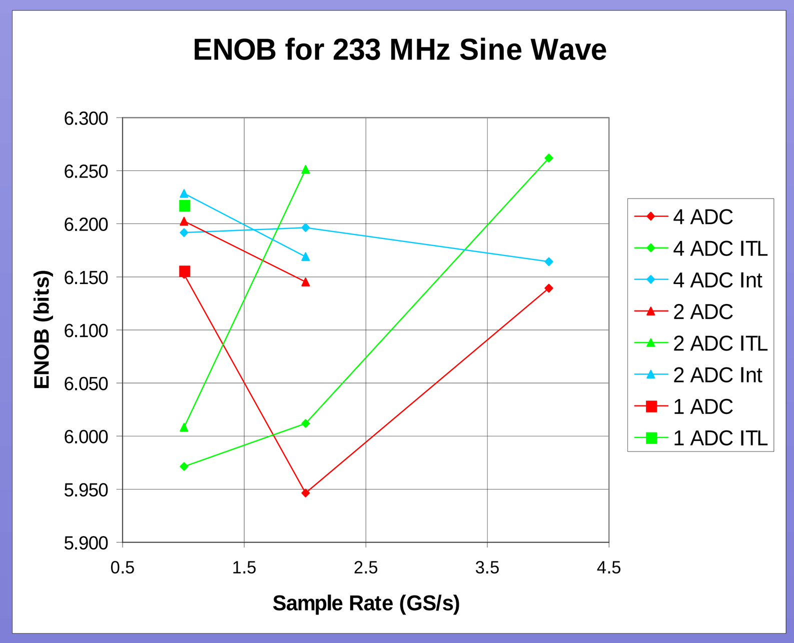
Compensation Results:

- With compensation, better ENOB is possible at higher sample rates
- With Int compensation, ENOB is roughly constant and independent of number of ADCs or sample rate
- TL compensation works poorly at low sample rates relative to signal frequency because slope estimate is poor

Technique	ENOB
Raw Data	6.139
TL	6.247
ITL	6.261
Int	6.165
Int + TL	6.276



Compensation results of 233 MHz sine wave



Summary of compensation results

Conclusions and Future Work:

- Our model captures the behavior of a digitizer well
- Compensation techniques based on this model improves ENOB
- Incorporate two tone transition level extraction method (Acunto, Arpaia, Hummels, and Irons 2001)

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